### Xcelera-CL VX4 Full





#### **Features**

- Half-length PCI Express x4 Board
- Acquires images from one Base, Medium or Full Camera Link®
- Real-time FPGA based hardware processing
- User programmable FPGA tools
- Supports Camera Link operations up to 85MHz
- Extended feature set supports advanced Camera Link pixel/tap configurations
- Windows® XP and Windows 7 (32/64-bit) compatible
- Fully Supported by Sapera APF and Sapera Vision Software SDKs
- FCC, CE and ROHS compliant

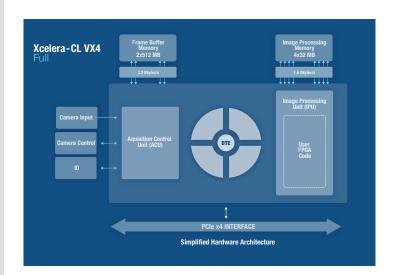
# Xcelera-CL VX4 Full - Next Generation Vision Processor Boards

The Xcelera-CL VX4 is the next generation user programmable vision processor based on the PCI Express X4 platform. It features powerful embedded processing architecture for real-time high-performance machine vision applications. Combining high-speed image acquisition capability with user programmable FPGAs (Field Programmable Gate Array) and graphical FPGA development tools, our vision processors deliver unmatched power and flexibility in real-time image processing on the PCIe platform.

The X64 Xcelera-CL VX4 Full is a Camera Link vision processor that is based on the PCI Express x4 interface. Compatible with a Base, Medium or Full Camera Link\* camera, the X64 Xcelera-CL VX4 Full supports a wide variety of multi-tap area and line scan colour and monochrome cameras. The X64 Xcelera-CL VX4 Full board can interface with advanced Camera Link cameras output formats including 10-taps of 8-bit at 85MHz pixel clock rates.

#### **Sophisticated Embedded Processing Platform**

The Xcelera-CL VX4 Full feature an FPGA hardware processing platform that combines ACU(Acquisition Control Unit), DTE (Data Transfer Engine) and IPU (Image Processing Unit) and state of the memory architecture. As a result, models such as our new Xcelera-CL VX4 are capable of handling variety of complex, real-time image processing topologies including iterative processing loops. While the FPGA technology provides ability to adapt to variety of high-speed, compute-intensive real-time processing applications, the Xcelera VX4 hardware design has been implemented using standard off-the-shelf components with long term availability.





## Xcelera-CL VX4 Full

Function	Description	Function	Description
Board	Camera Link Specifications Rev 1.2 compatible Half length PCI Express 1.1 x4 compliant ROHS Compliant	Controls	Comprehensive event notification includes start/end of frame/transfer Camera control signals for external event synchronization Optically isolated trigger inputs
Acquisition	Supports one Base, Medium or Full Camera Link area and line scan camera Acquisition pixel clock rates from 20MHz to 85MHz		programmable as active high or low (edge or level trigger) TTL Strobes outputs PC independent serial communications
Resolution	Horizontal Size (min/max): 16 byte/64K bytes  Vertical Size (min/max):  1 line/infinite lines for line-scan cameras		ports provide support 9600 to 11500K baud Appears as system serial ports enabling seamless interface to host applications
	1 line/inimite lines for line-scan carrieras 1 line/16million lines/frame for area-scan cameras Variable length frame size from 1 to 16 million lines for area-scan Cameras	Encoder Inputs	Optically isolated quadrature (AB) shaft-encoder inputs for external web synchronization
	2x512MB onboard frame buffer memory 4x32MB image processing memory	On-board GPI/Os'	4-optically isolated general purpose inputs tolerate 5 and 24VDC signals4 general purpose outputs
	Integrated advanced tap reversal engine allows independent tap formatting		Power-on-reset fused +12V output @ 1.5A
Pixel Format and Tap	Supports Camera Link tap configurations	Power Output	+5V DC output at 1.5A
configuration	for 8, 10, 12, 14 and 16-bit mono or 8, 10 or 12-bit RGB For Base cameras in any of the following combinations: 3x8-bit/tap, 2x10-bits/tap, 2x12-bit/tap, 1x14-bit/tap, 1x16-bits/tap, & 1x24-bit/RGB For Medium camera - 4x8-bit/tap, 4x10-bits/tap, 4x12-bit/tap, 1x30-bit/RGB, & 1x36-bits/	Software	Device driver supports: Microsoft Windows XP and Windows 7 (32/64-bit) compatible Fully supported Teledyne DALSA's Sapera Vision Software packages Application development using C++ and .Net languages(C++, C# or Visual Basic)
	tap For Full—8x 8-bit/tap Camera Link; 10-tap/8-bit and 8-tap/10-bit configurations	System Requirements	PCI Express Rev 1.1 compliant with one x4 slot system with 1024MB or higher system memory
		Dimensions	6.375" (16.1cm) Length X 4.20" (10.7 cm) Height
		Temperature	10°C (50° F) to 50° C (122° F)
			Relative Humidity: up to 90% (non- condensing)
		Markings	FCC Class B – Approved CE—Approved
www.teledynedalsa.com		Requires a separate slot for the bracket assembly	

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